REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 3, 5, 8-9, 12, 14, 17-20, 23-26, 28-33, and 37-40 are in this application. Claims 1-2, 4, 6-7, 10-11, 13, 15-16, 21-22, 27, and 34-36 have been cancelled. Claims 3, 5, 8, 9, 12, 14, 17-20, 23, and 24 have been allowed. Claim 25 has been amended.

In the Office Action dated November 28, 2005, the Examiner presented new grounds of rejection in finally rejecting claims 25, 26, 28, 30, 31, and 37-40. Applicant filed an after-final response on January 30, 2006 discussing the patentability of the claims in view of the new grounds of rejection. In the Advisory Action, the Examiner did not respond to applicant's comments, but merely indicated that the Examiner believed the rejections to be correct.

Applicant respectfully notes that applicant can not further prosecution without specific comments from the Examiner as to why the Examiner believes that the rejections are correct. Since the after-final response was entered only for the purposes of appeal, applicant has filed an RCE with the present amendment, which repeats substantial portions of the after-final response, and requests the Examiner to discuss applicant's arguments with respect to the patentability of the claims.

The Examiner rejected claims 25-26 and 28 under 35 U.S.C. §102(b) as being anticipated by Hmida et al. (U.S. Patent No. 4,920,509). Claim 25 has been amended, not to overcome the Hmida reference, but to further prosecution by expressly reciting the limitations of the transmission gates. As discussed in the after-final amendment, the gates of the transistors of the transmission gates could not have been read to be the inputs of the transmission gates. Thus, for the reasons set forth below, applicant respectfully traverses this rejection.

Claim 25 recites:

"a first adder cell having:

"a first exclusive OR circuit having a first input, a second input, and an output, the output having a logic state that represents an exclusive ORing of a logic state on the first input and a logic state on the second input;

"a first output circuit having:

"a first transmission gate having an input, an output, a first transistor, and a second transistor, the first transistor having a first terminal connected to the input of the first transmission gate, a second terminal connected to the output of the first transmission gate, and a first gate electrically isolated from the first and second terminals, the second transistor having a first terminal connected to the input of the first transmission gate, a second terminal connected to the output of the first transmission gate, and a second gate electrically isolated from the first and second terminals of the second transistor;

"a second transmission gate having an input, an output, a first transistor, and a second transistor, the first transistor of the second transmission gate having a first terminal connected to the input of the second transmission gate, a second terminal connected to the output of the second transmission gate, and a first gate electrically isolated from the first and second terminals of the first transistor of the second transmission gate, the second transistor of the second transmission gate having a first terminal connected to the input of the second transmission gate, a second terminal connected to the output of the second transmission gate, and a second gate electrically isolated from the first and second terminals of the second transistor of the second transmission gate, the outputs of the first and second transmission gates being connected together;

"a third transmission gate having an input, an output, a first transistor, and a second transistor, the first transistor of the third transmission gate having a first terminal connected to the input of the third transmission gate, a second terminal connected to the output of the third transmission gate, and a first gate electrically isolated from the first and second terminals of the first transistor of the third transmission gate, the second transistor of the third transmission gate having a first terminal connected to the input of the third transmission gate, a second terminal connected to the output of the third transmission gate, and a second gate electrically isolated from the first and second terminals of the second transistor of the third transmission gate;

"a fourth transmission gate having an input, an output, a first transistor, and a second transistor, the first transistor of the fourth transmission gate having a first terminal connected to the input of the fourth

transmission gate, a second terminal connected to the output of the fourth transmission gate, and a first gate electrically isolated from the first and second terminals of the first transistor of the fourth transmission gate, the second transistor of the fourth transmission gate having a first terminal connected to the input of the fourth transmission gate, a second terminal connected to the output of the fourth transmission gate, and a second gate electrically isolated from the first and second terminals of the second transistor of the fourth transmission gate, the outputs of the third and fourth transmission gates being connected together; and

"a first inverting circuit having an input connected to the input of the second transmission gate and the input of the third transmission gate, and an output connected to the input of the fourth transmission gate."

In rejecting the claims, the Examiner pointed to exclusive OR gate 2200 shown in FIG. 8 of Hmida as constituting the exclusive OR gate required by claim 25, modules 2400 and 2800 shown in FIG. 8 of Hmida as constituting the first output circuit required by claim 25, and inverter 2500 shown in FIG. 8 of Hmida as constituting the first inverting circuit required by claim 25.

Inverter 2500 shown in FIG. 8 of the Hmida et al. reference, however, can not be read to be the first inverting circuit required by claim 25 because inverter 2500 does not have an input connected to the inputs of the second and third transmission gates, and an output connected to the input of the fourth transmission gate.

In the following discussion, it is assumed that the Examiner has read the lower and upper transmission gates in module 2400 to be the first and second transmission gates, respectively, required by claim 25, and the lower and upper transmission gates in module 2800 to be the third and fourth transmission gates, respectively, required by claim 25. It is further assumed that the Examiner has read the first transistor of the first transmission gate to be the left-side transistor, and the second transistor of the first transmission gate to be the right-side transistor.

As shown in FIG. 8 of Hmida, inverter 2500 has an input and an output that are connected to the gates of the lower and upper transmission gates in module 2400 (assumed to be read to be the first and second transmission gates required by

claim 25), and the gates of the lower and upper transmission gates in module 2800 (assumed to be read to be the third and fourth transmission gates required by claim 25).

Thus, although inverter 2500 is connected to the gates, the input of inverter 2500 is not connected to the input of the upper transmission gate in module 2400 (assumed to be read to be the second transmission gate) and the input of the lower transmission gate in module 2800 (assumed to be read to be the third transmission gate). In addition, inverter 2500 does not have an output that is connected to the input of the upper transmission gate in module 2800 (assumed to be read to be the fourth transmission gate). As a result, inverter 2500 does not have an input and an output that are connected to the transmission gates as required by claim 25.

Thus, since the Hmida reference fails to teach or suggest an inverting circuit as required by claim 25, claim 25 is not anticipated by Hmida et al. In addition, since claims 26 and 28 depend either directly or indirectly from claim 25, claims 26 and 28 are not anticipated by Hmida for the same reasons as claim 25.

The Examiner also rejected claims 30-31 and 37-40 under 35 U.S.C. §103(a) as being unpatentable over Hmida et al. In rejecting the claims, the Examiner argued that Hmida teaches all of the limitations of claim 25. However, as noted above, Hmida does not teach all of the limitations of claim 25. Thus, since Hmida does not teach all of the limitations of claim 25, claims 30-31 and 37-40 are patentable over Hmida for the same reasons that claim 25 is not anticipated by Hmida.

The Examiner objected to claims 29 and 32-33 as being dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten to be in independent form to include all of the limitations of the base claim and any intervening claims. However, in view of the above discussion, claims 29 and 32-33 have not been amended at this time.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are requested.

Respectfully submitted,

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